

Editing Compact Voxel Representations on the GPU

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Delft University of Technology







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Sparse Voxel Octree

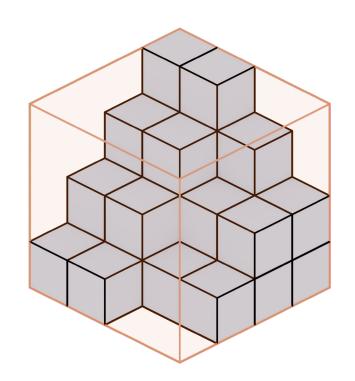


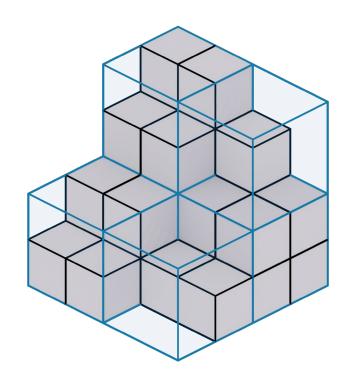
Voxel Octree

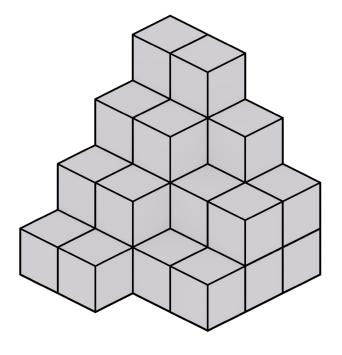
Recursively subdivide space into evenly sized 2³ regions

Sparse

Don't subdivide empty regions









Sparse Voxel Octree

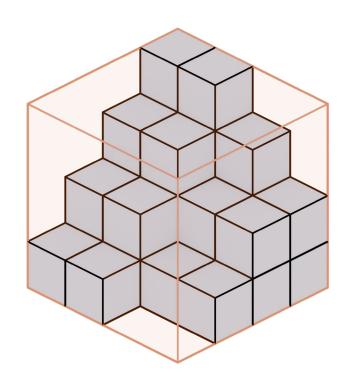


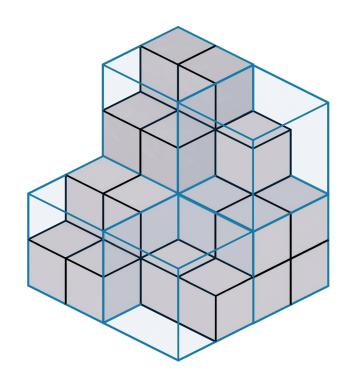
Voxel Octree

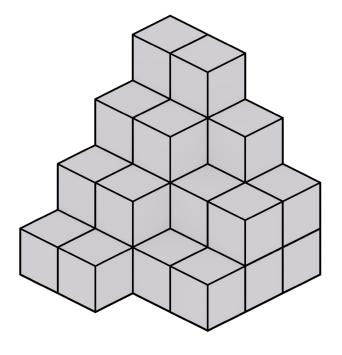
Recursively subdivide space into evenly sized 2³ regions

Sparse

Don't subdivide empty regions



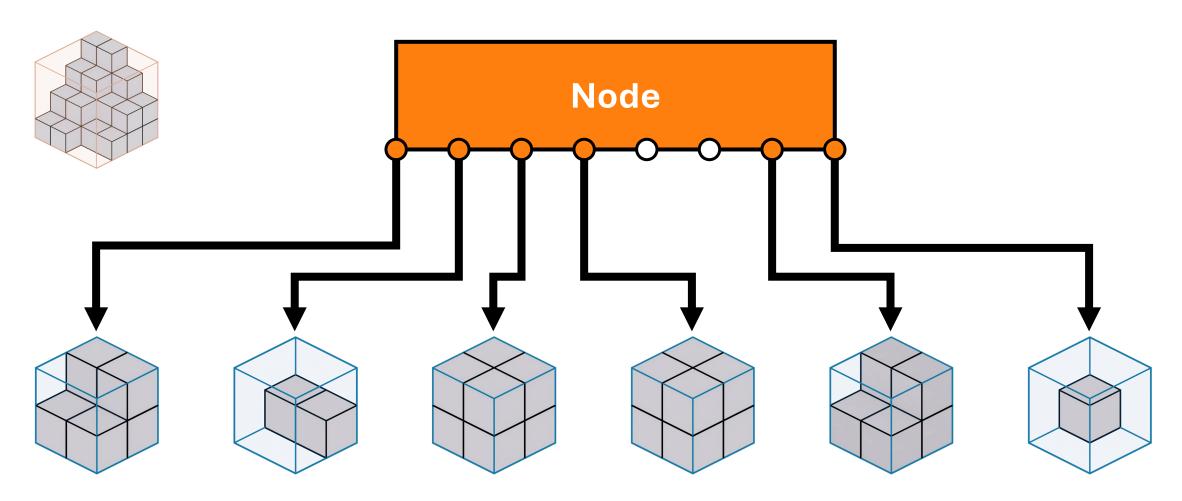




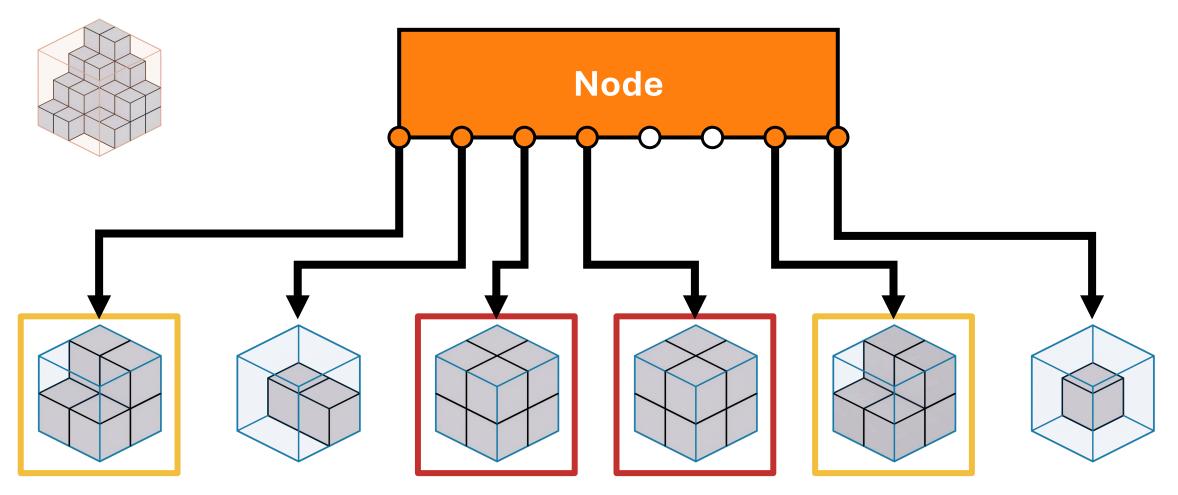


Sparse Voxel Octree (SVO)

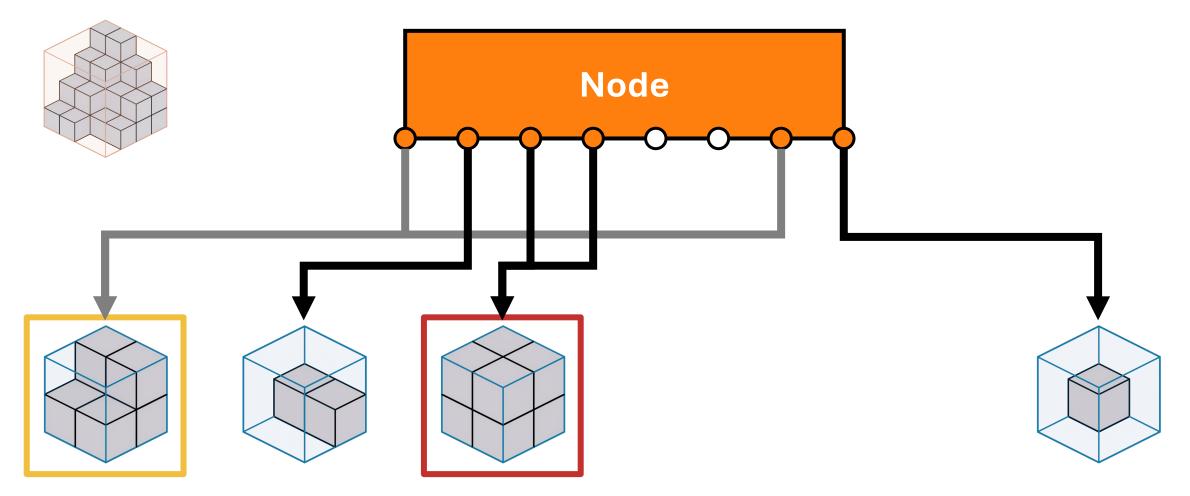




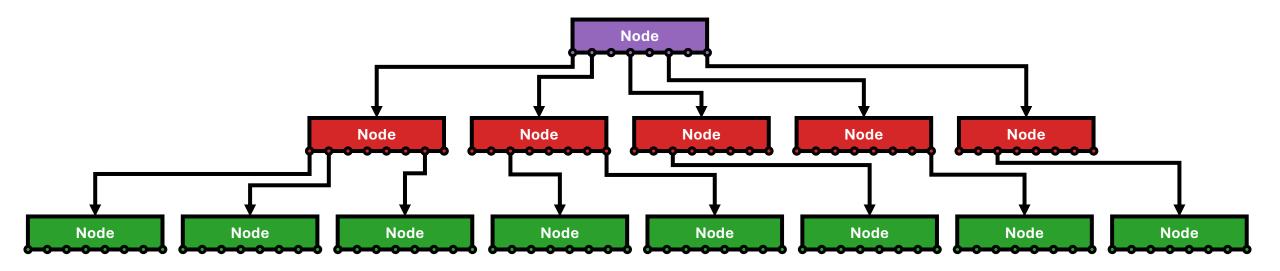


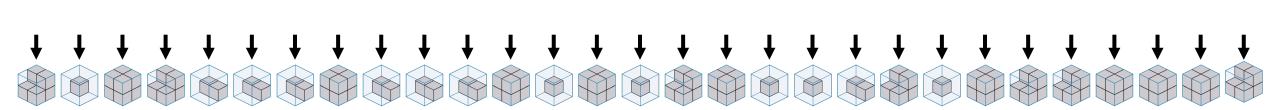






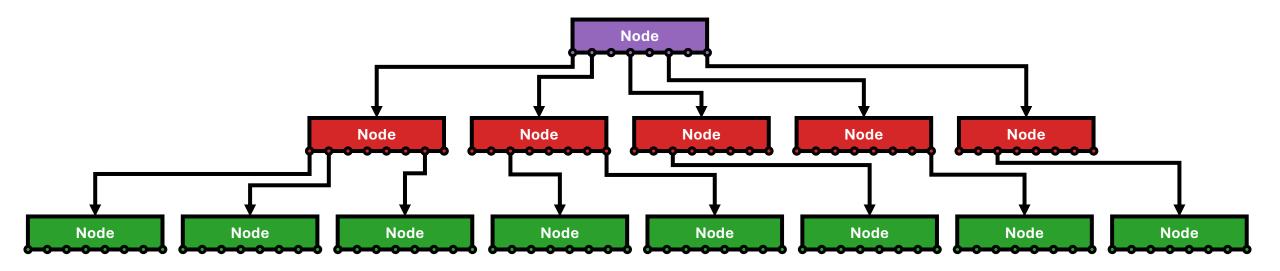


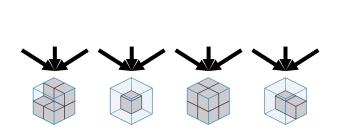






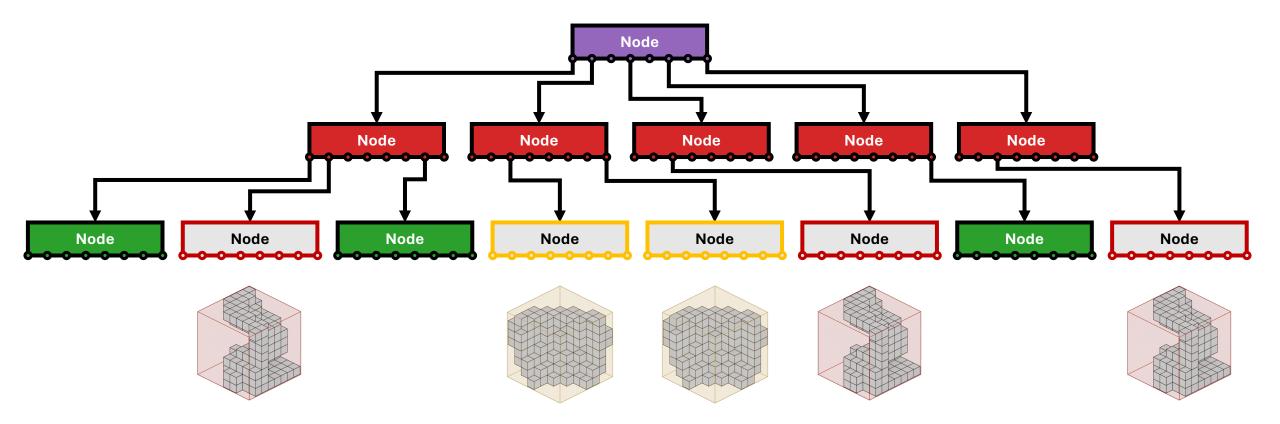






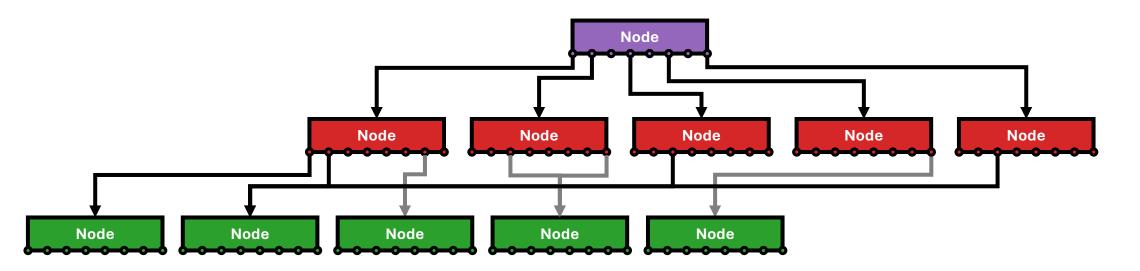


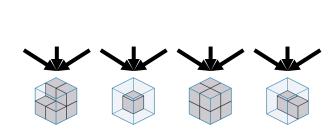






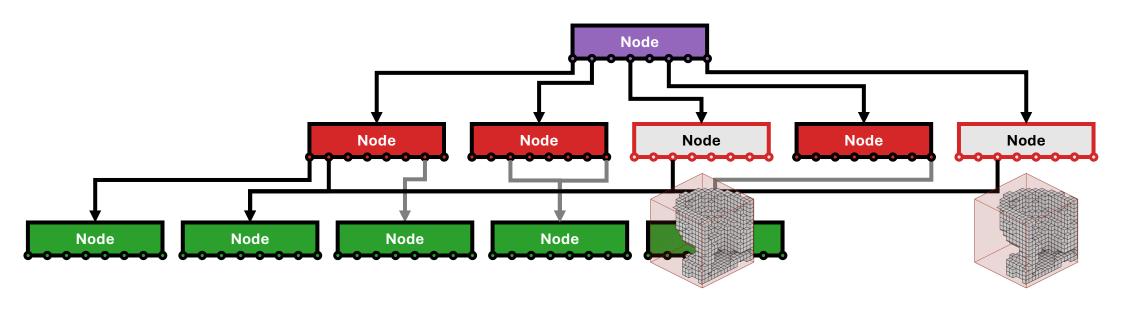


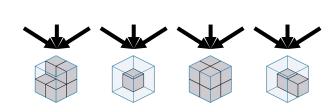






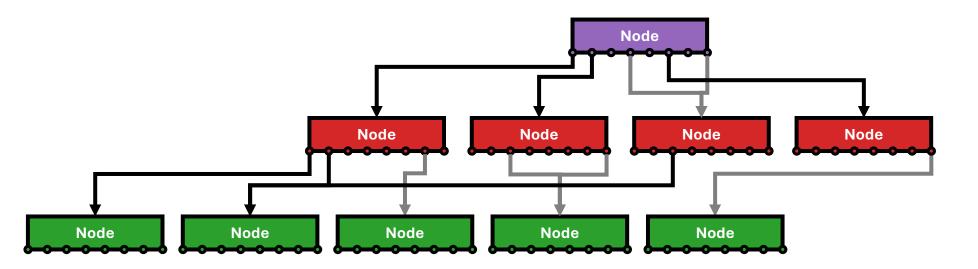


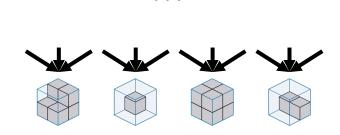






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Scene		SVO	SVDAG [KSA13]	
Citadel 128K³ (No Materials) 13.7B occupied voxels		15,117 MiB	980 MiB	15.4x
Citadel 128K ³ (4-bit Materials) 13.7B occupied voxels		22,516 MiB	5,997 MiB	3.7x
San Miguel 64K³ (4-bit Materials) 10.3B occupied voxels		14,865 MiB	2,929 MiB	5.0x



Editing Compact Voxel Representations on the GPU

HashDAG [CBE20]

Make modifications to existing SVDAG file

Performance considerations

Editing CPU (Multi Threaded)

Rendering GPU



EUROGRAPHICS 2020 / U. Assarsson and D. Panozzo (Guest Editors) Volume 39 (2020), Number 2

Interactively Modifying Compressed Sparse Voxel Representations

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¹Delft University of Technology, The Netherland ²Université de Rennes, France



Figure 1: To test and demonstrate our method for editing large sparse voxel geometries, we have implemented an interactive prototype application with support for interactive editing operations. The left image shows a copy operation in the Epic Citadel scene, voxelized at an resolution of (1288). The statue intelled this building contains show 170% voxels: The middle mape shows large scale edits, copying an eiter building (order of 80M voxels). The right images illustrate tools so add and delete voxels, as well as paint voxel color attributes. The bottom right image uses the Sam Migual model, voxelized at Geld³), where we first soldified, then covered a hole in a column.

stract

Vacels are a popular choice to encode complex geometry. Their regularity makes updates easy and enables random retrieval of values. The main limitation lies in the poor scaling with respect to resolution. Sparse vived InGG (Directed Acyclic Graphs) overcome this handle and offer high-resolution representations for real-time rendering but only handle static data. We introduce a novel data structure to enable interactive modification of such compressed vived geometry without requiring de- and recompression. Besides binary data to encode geometry, it also supports compressed attributes (e.g., color). We illustrate the usefulness of our representation via an interactive large-scale voxel editor (supporting carring), fifting, copying, and painting).

CCS Concepts

Computing methodologies → Volumetric models;

1. Introductio

Compressed sparse voxel structures have gained popularity as an alternative representation for highly-detailed geometry. Woxel-based approaches encode the scene as a high-resolution grid, where cells ("voxels") hold information to define the scene. While naively storing such grids is infeasible for large resolutions, hierarchical representations can exploit sparsity [MeaS2] and similarity

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© 2020 The Author(s) Computer Graphics Forum © 2020 The Eurographics Association and Joh [KSA13, JMG16, KRB*16] to achieve significant compression rates. Kämpe et al. [KSA13] demonstrate (128k)* resolutions at less than 1GB, while still enabling real-time rendering of this compressed form. Originally, such DAG (directed acyclic graph)based structures only encoded solid geometry, however, later works [DKB*16, DSKA18] extend the methods to include compressed per-vocal attributes, such as color.

Until now, sparse voxel DAG structures are pre-built in a separate, often off-line, construction step, which limits their use to static elements. We introduce a solution to dynamically modify sparse voxel







Hash table size heuristically determined at start-up:

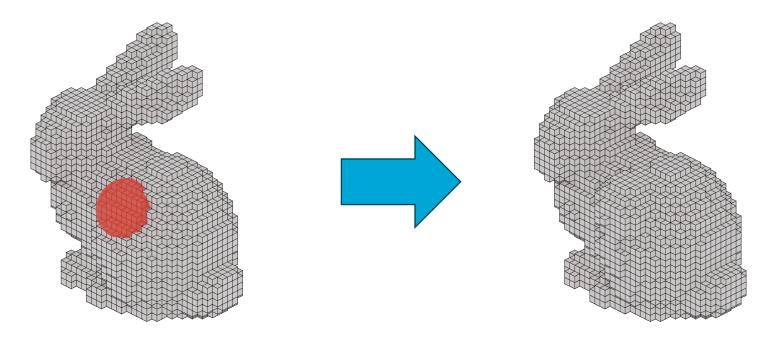
- Number of buckets
- Maximum size of each bucket

Custom virtual memory system to store the hash table.





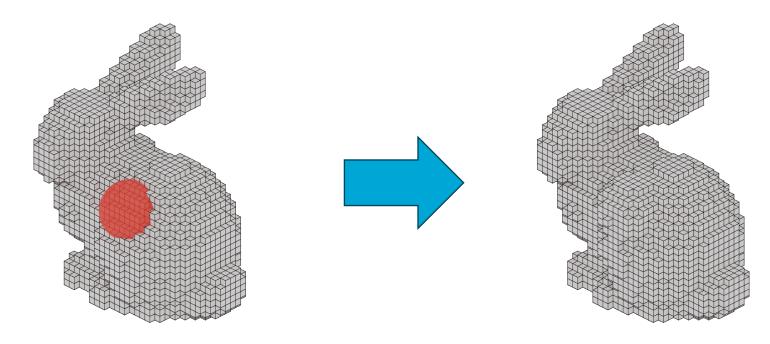
- Limited scalability due to mutex locking
- CPU → GPU copy of scattered data
- Designed for local edits







- Limited scalability due to mutex locking
- CPU → GPU copy of scattered data
- Designed for local edits





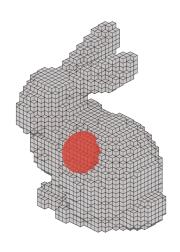


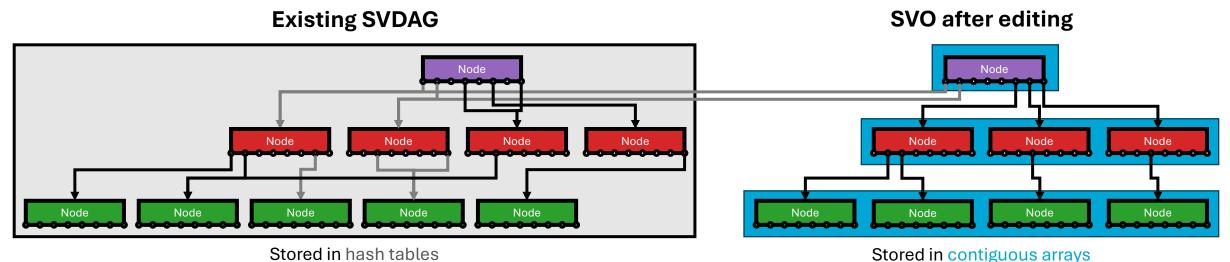
Our Work

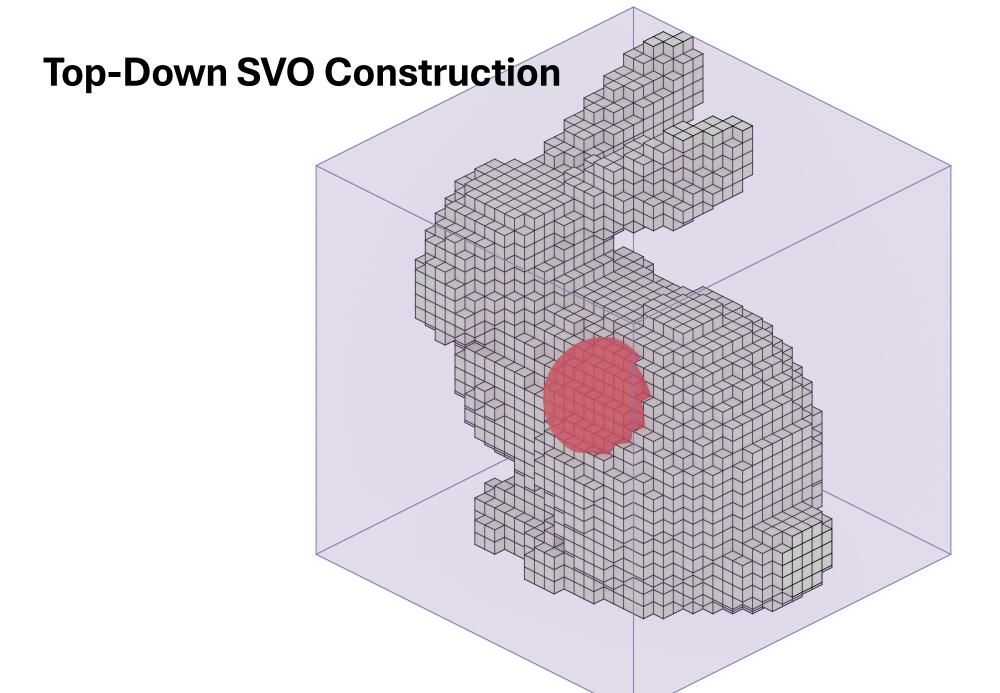
Editing on the GPU



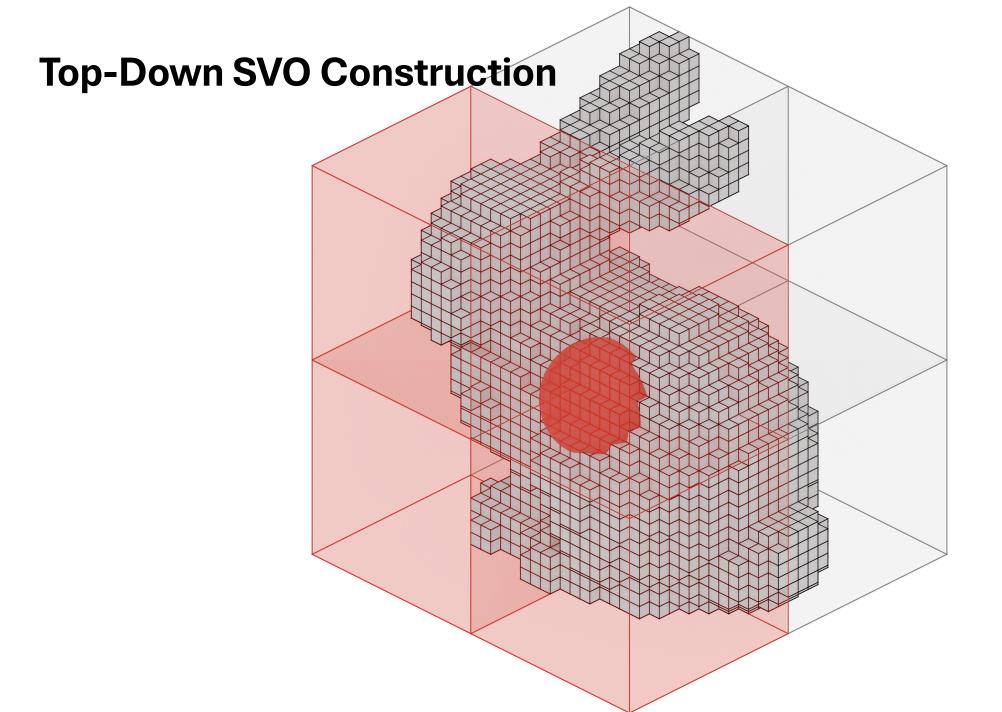
- 1. Construct a Sparse Voxel "Octree" of the modified scene
 - Point to existing SVDAG for unchanged regions







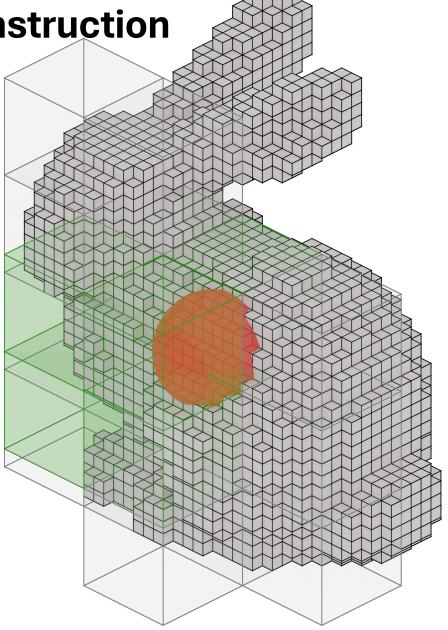






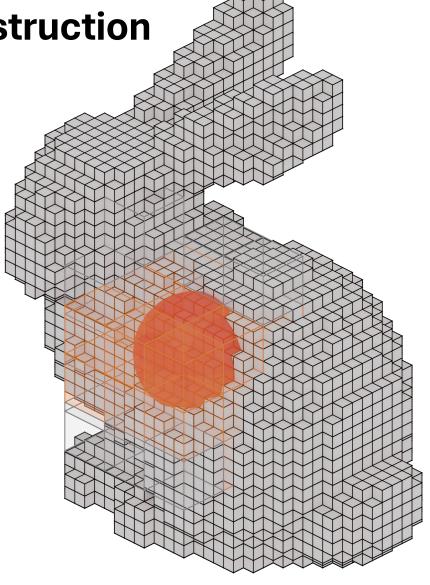
Top-Down SVO Construction





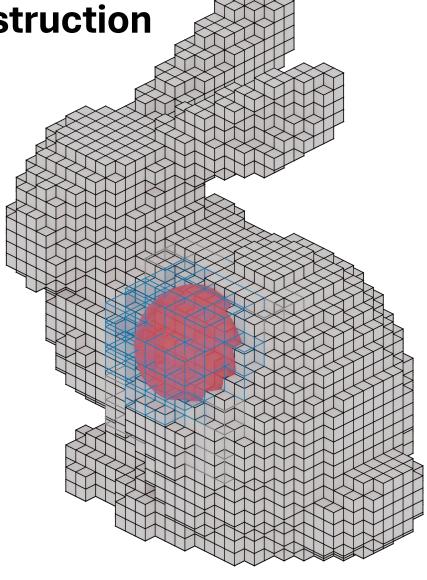






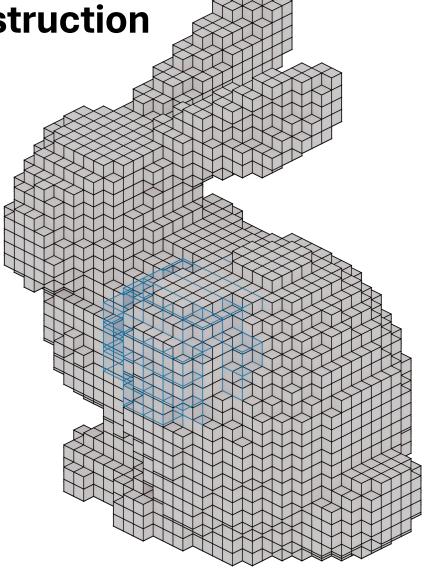




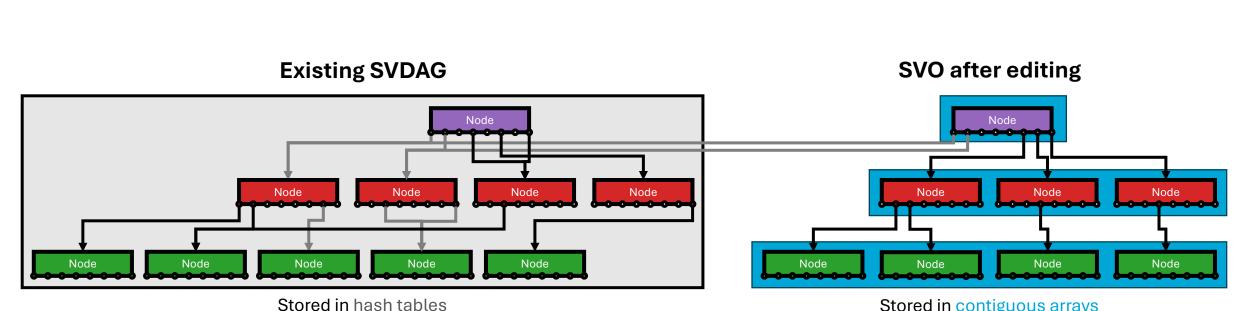






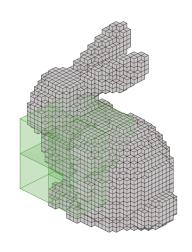


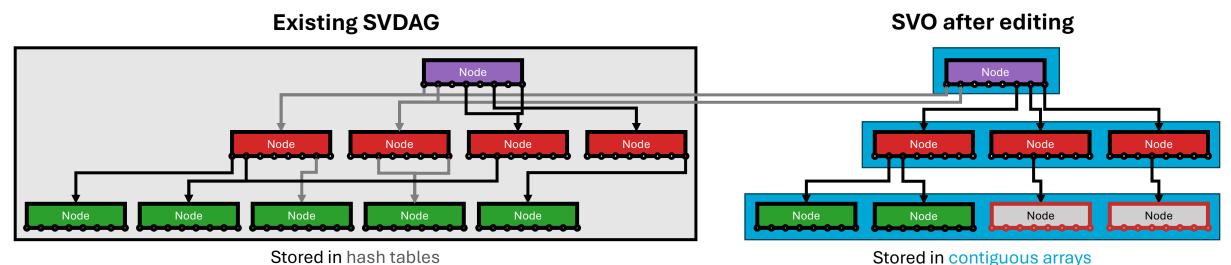
- 1. Construct a Sparse Voxel "Octree" of the modified region
- 2. Remove duplicates within this Octree
 - Use hash table to find duplicates



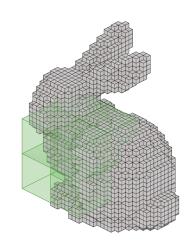
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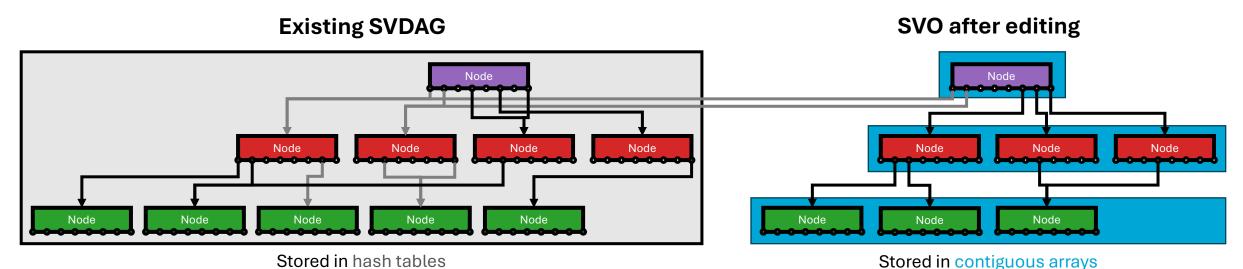
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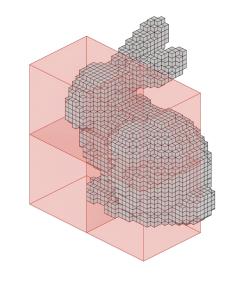


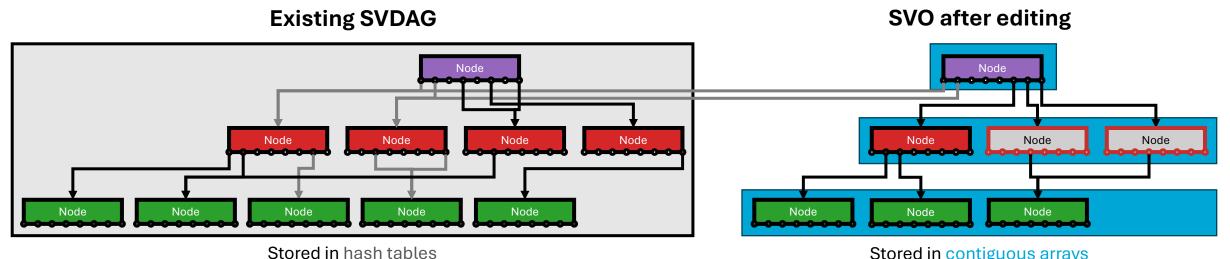
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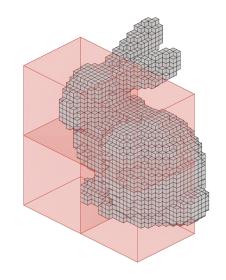
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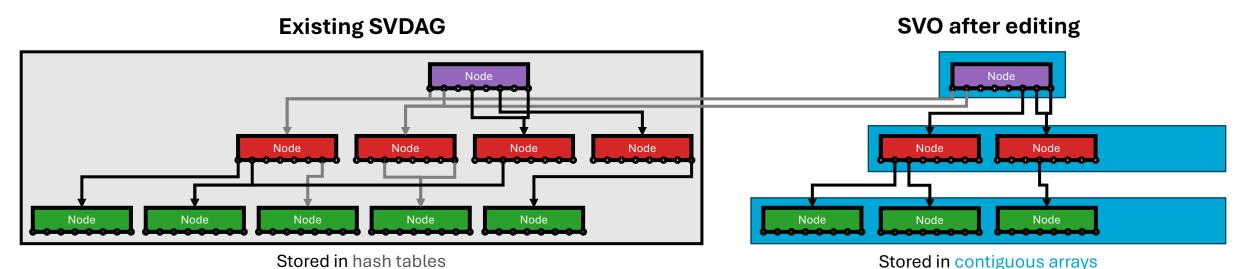




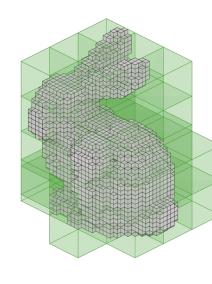
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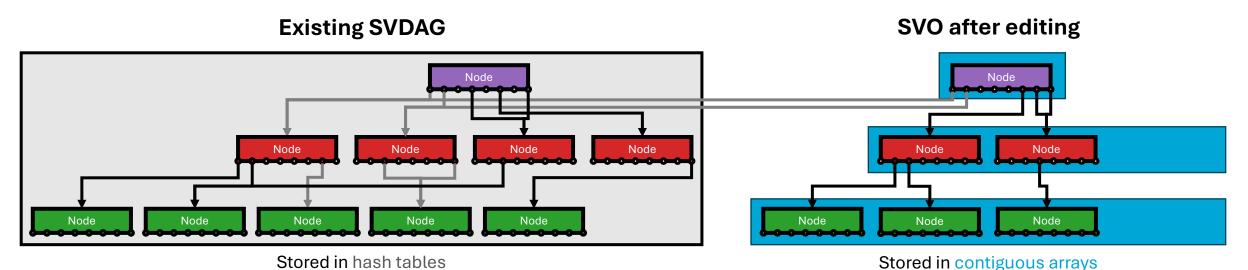
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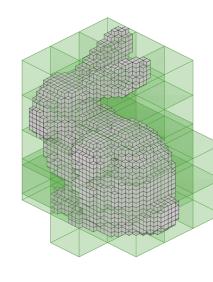


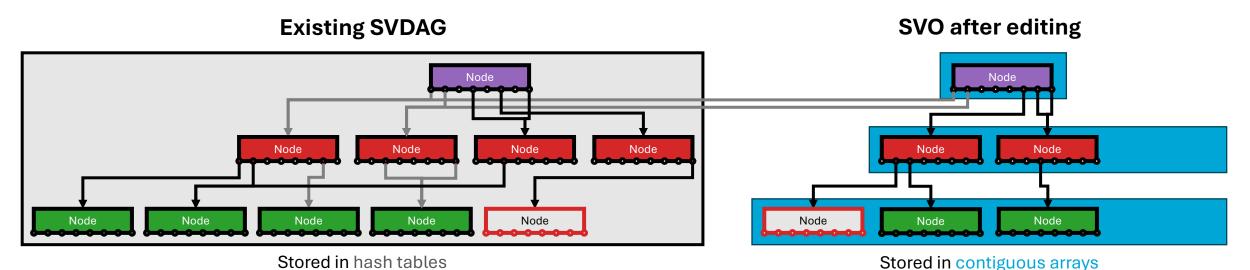
- 1. Construct a Sparse Voxel "Octree" of the modified region
- 2. Remove duplicates within this Octree
- 3. Merge into existing SVDAG



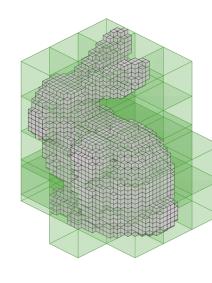


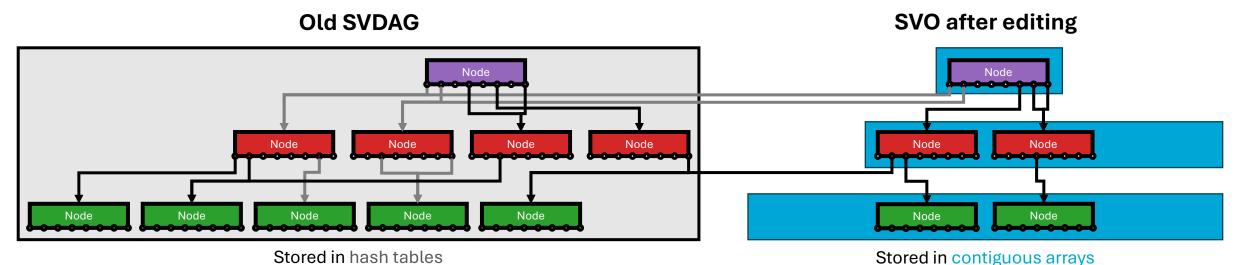
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- 1. Construct a Sparse Voxel "Octree" of the modified region
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- 3. Merge into existing SVDAG

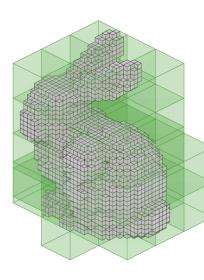




Conceptual Overview

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- 1. Construct a Sparse Voxel "Octree" of the modified region
- 2. Remove duplicates within this Octree
- 3. Merge into existing SVDAG









GPU Hash Table

SlabHash [AFC018]

Matches most of our requirements:

- Optimized for the GPU
- Pointer stability under insertion
- Must support "large" items (>64 bits)



2018 IEEE International Parallel and Distributed Processing Symposium

A Dynamic Hash Table for the GPU

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Electrical and Computer Engineering

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Abtrace—We design and implement a fully concurrent of upmanic hash table for GPUs with comparable performance to the state of the art static hash tables. We propose a warp-cooperative work sharing strategy that reduces branch divergence and provides an efficient alternative to the traditional way of per-thread (or per-varp) work assignment and processing. By using this strategy, we build a dynamic non-blocking concurrent linked link to stab link at supports as well as search queries. We use the slab list to implement a dynamic hash table with chaining (the slab hash). On an NVIDIA Tesla K40c GPU, the slab hash performs updates with up to 512 M updates and processes search queries with up to 937 M queries/s. We also design a warp-synchronous dynamic mency allocator, Niskelifice, that sults the high performance memory allocator, Niskelifice, that sults the high performance needs of the slab hash, ShabAlloc dynamically allocates memory alternatives methods in similar scenarios.

I. INTRODUCTION

A key deficiency of the GPU ecosystem is its lack of dynamic data structures, which allow incremental updates (such as insertions and deletions). Instead, GPU data structures (e.g., cuckoo hash tables [11] typically address incremental Changes to a data structure by rebuilding the entire data structure from scratch. A few GPU data structures (e.g., the dynamic graph data structure in cuSTINGER [21] implement phased updates, where updates occur in a different execution phase than lookups. In this work we describe the design and implementation of a hash table for GPUs that supports truly concurrent insertions and deletions that can execute loogether with lookups.

Supporting high-performance concurrent updates of data structures on GPUs support tens of thousands of simultaneous resident threads, so traditional lock-based methods that enforce concurrency will suffer from substantial contention and will thus likely be inefficient. Non-blocking approaches offer more potential for such massively parallel frameworks, but most of the multi-core system literature (e.g., classic non-blocking linked lists [3]) neglects the sensitivity of GPUs to memory access patterns and branch divergence, which makes it inefficient to directly translate those ideas to the CBH.

In this paper, we present a new GPU hash table, the slab

hash, that supports bulk and incremental builds. One might expect that supporting incremental insertions and deletions would result in significantly reduced query performance compared to static data structures. However, our hash table not only supports updates with high performance but also sustains build and query performance on par with static GPU hash tables. Our hash table is based on a novel linked list data structure, the slab list, Previous GPU implementations of linked lists [4], which operate on a thread granularity and contain a data element and pointer per linked list node. exhibit poor performance because they suffer from control and memory divergence and incur significant space overhead. The slab list instead operates on a warp granularity, with a width equal to the SIMD width of the underlying machine and contains many data elements per linked list node. Its design minimizes control and memory divergence and uses space efficiently. We then construct the slab hash from this slab list as its building block, with one slab list per hash bucket. Our contributions in this work are as follows:

- The slab list is based on a node structure that closely matches the GPU's hardware characteristics.
- The slab list implementation leverages a novel warp-cooperative work sharing strategy that minimizes branch divergence, using warp-synchronous programming and warp-wide communications.
- The slab hash, based on the slab list, supports concurrent operations with high performance.
- To allow concurrent updates, we design and implement a novel memory allocator that dynamically and efficiently allocates and deallocates memory in a way that is well-matched to our underlying warp-cooperative implementation.
- Our memory allocator is scalable, allowing us to support data structures up to 1 TB (far larger than the memory size of current GPUs) and without any CPU intervention.
- The slab hash's bulk-build and search rates are comparable to those of static methods (e.g., GPU cuckoo hashing [1]), while additionally achieving efficient incremental updates.

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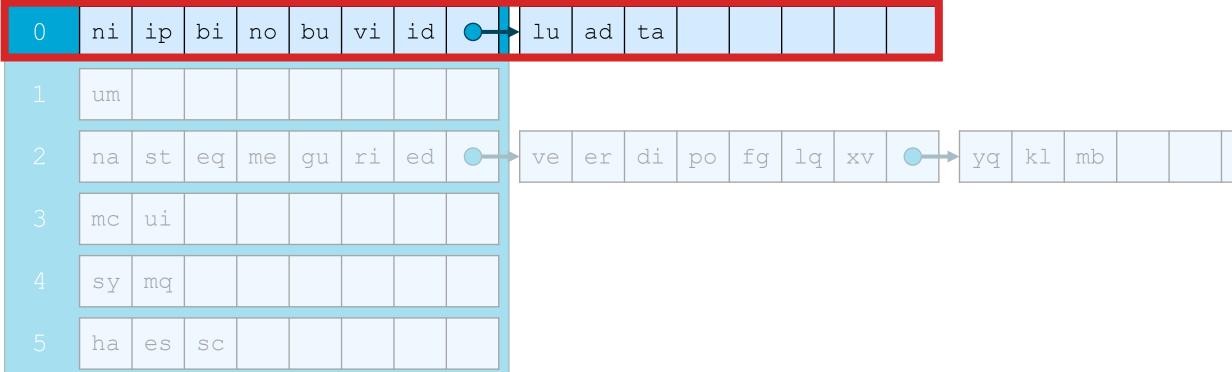


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SlabHash [AFCO18] - Terminology



Bucket

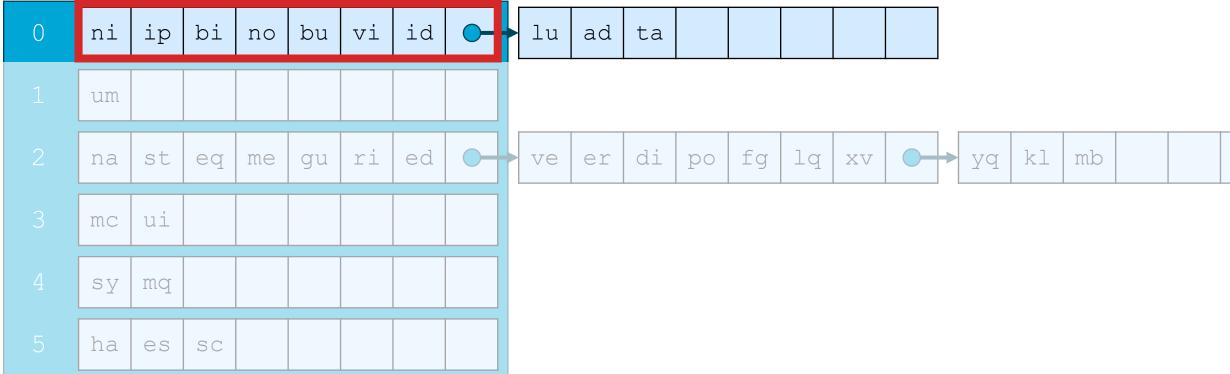


SlabHash [AFCO18] - Terminology



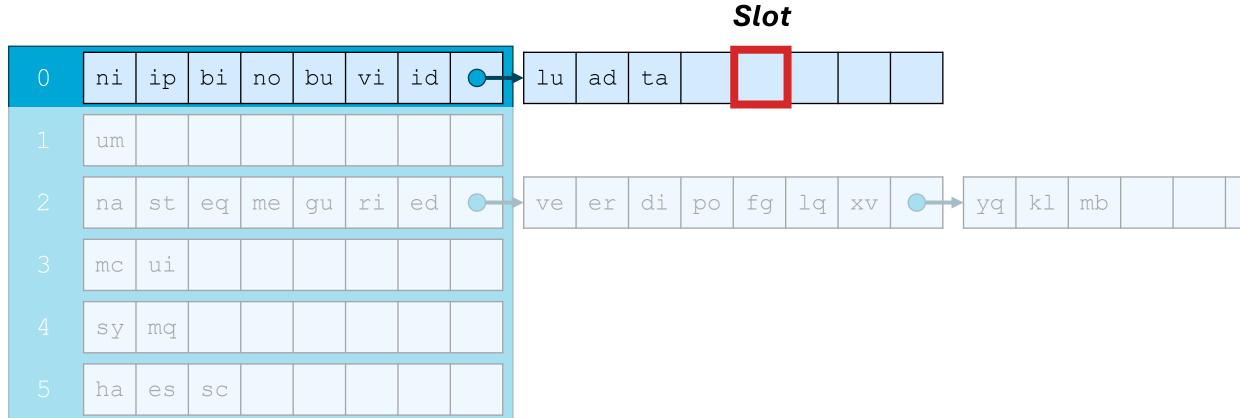
Linked list of 32-slot groups (aka *slabs*)

Shown as slabs of 8 slots for brevity



SlabHash [AFCO18] - Terminology









Empty slots are indicated by a reserved special value (typically "0").

Atomically swapped with the to-be inserted item.

Supports multiple operations in parallel:

- Insertion
- Search
- Removal





Extending SlabHash





Extending SlabHash [AFCO18] to store large items (of uniform size)

We propose three hash table designs:

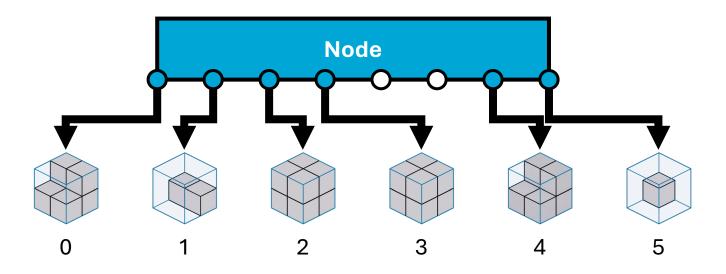
- 1. 64-bit Atomic Compare-and-Swap
- 2. Ticket Board
- 3. Acceleration Hash (both 8-bit and 32-bit)

Inner Node Encoding



- 32-bit header (8-bit child mask)
- 32-bit pointers to non-empty children

11110011 0 1 2 3 4 5

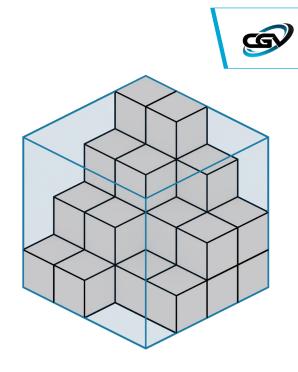




Leaf Encoding (4³ voxels)

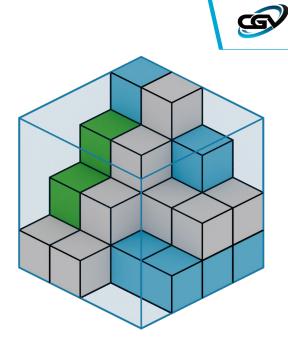
64-bit bitmask





Leaf Encoding (4³ voxels)

- 64-bit bitmask
- 4-bit material per occupied voxel



01010101	01010101	stone	grass	stone	ı
----------	----------	-------	-------	-------	---

W	ater	grass	grass	stone	water	water
---	------	-------	-------	-------	-------	-------





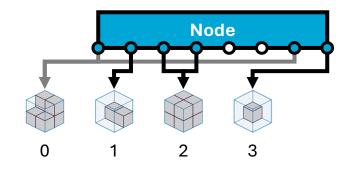
Note: items never start with 64-bit "0"

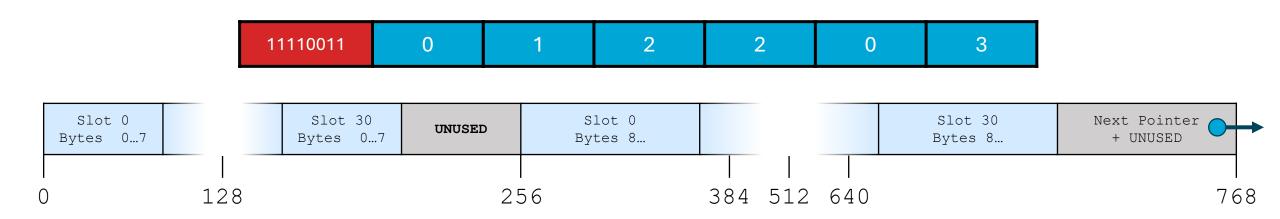
- Leaf must have at least 1 filled voxel
- Nodes must have at least 1 child

Atomically swap "0" to insert or remove



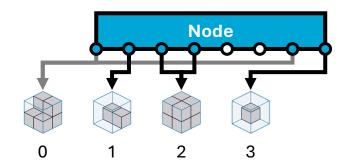
Store first 64 bits (8 bytes) of each slot

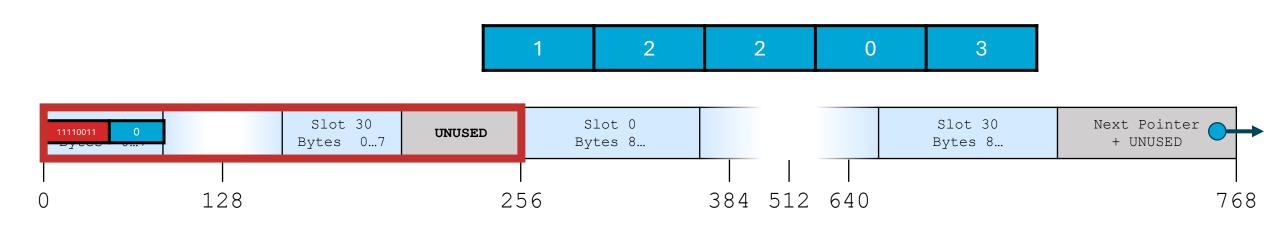






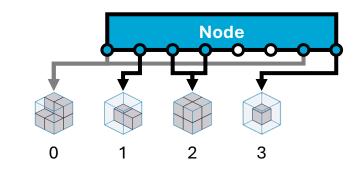
• Store first 64 bits (8 bytes) of each slot

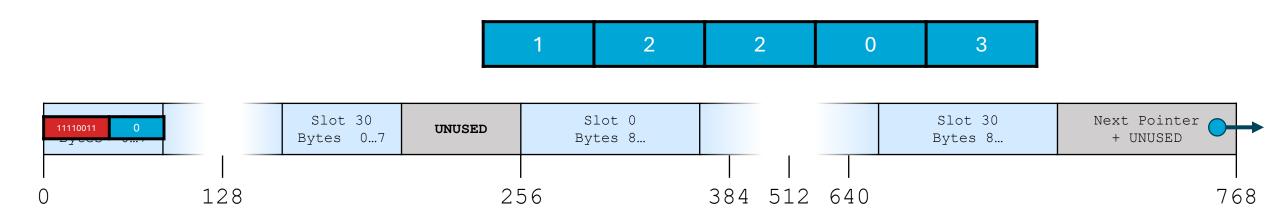






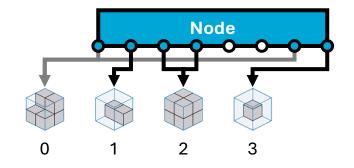
- Store first 64 bits (8 bytes) of each slot
- Store item remainders at the end of the slab

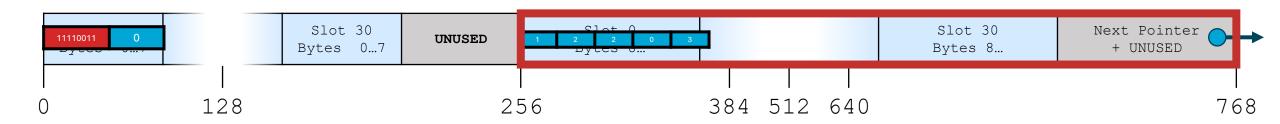






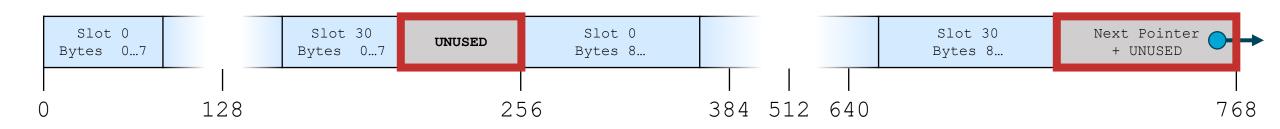
- Store first 64 bits (8 bytes) of each slot
- Store item remainders at the end of the slab







- Store first 64 bits (8 bytes) of each slot
- Store item remainders at the end of the slab
- 31 slots per slab to improve memory alignment

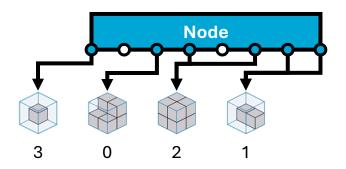


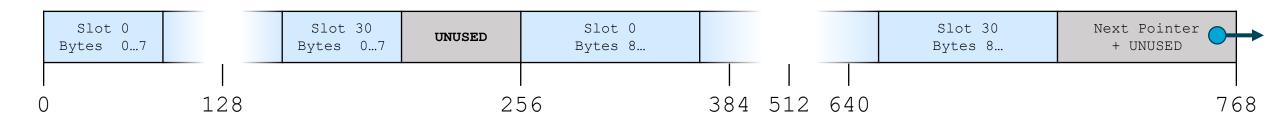
64-bit Atomic - Look-Up Efficiency



Search for the following node:



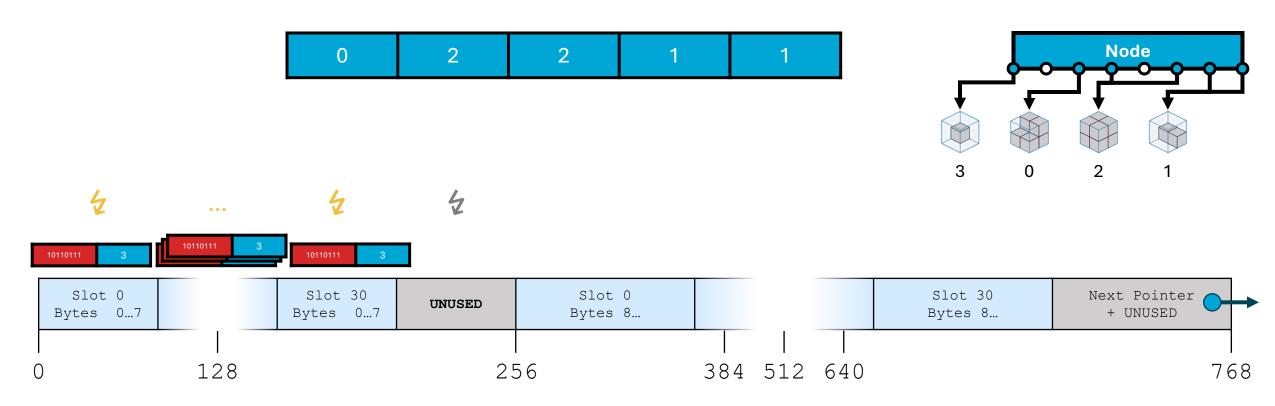








Warp of 32 threads to collaboratively check first 64-bits of each item

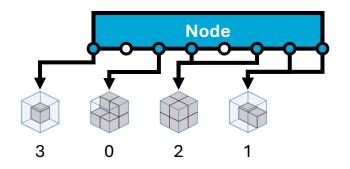


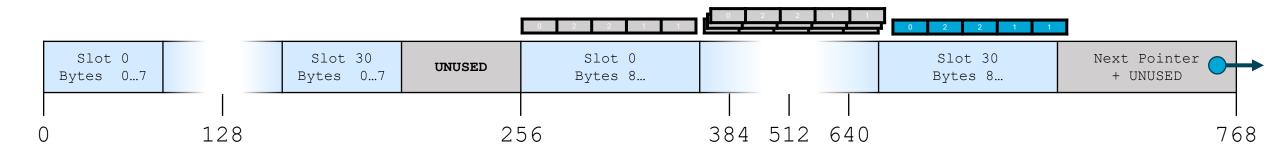




Warp of 32 & threads & collaboratively check first 64-bits of each item

Only test *remainder* for potentially matching slots

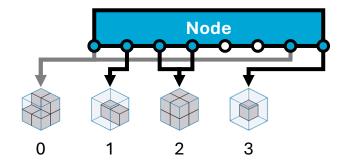


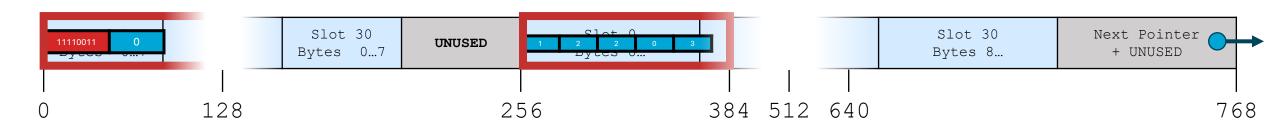




64-bit Atomic - SVDAG Traversal Performance

Visiting a node often requires loading two cache lines



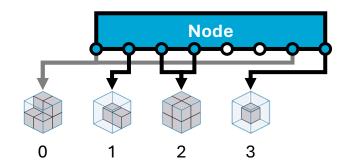


Ticket Board

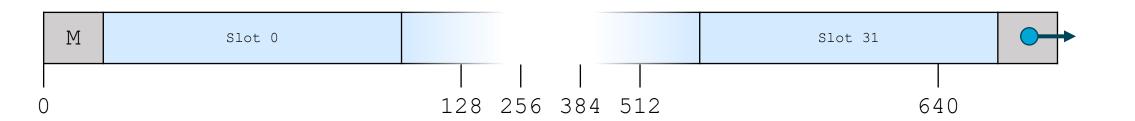


Inspired by Stadium Hashing [KBGB15]

- 32-bit mask M to indicate slot usage
- No alignment padding





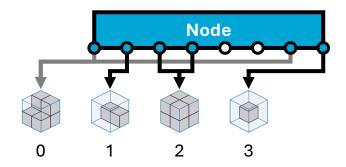


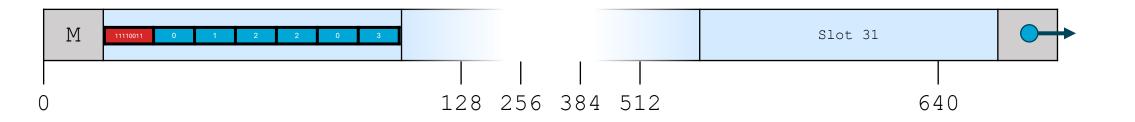
Ticket Board



Inspired by Stadium Hashing [KBGB15]

- 32-bit mask M to indicate slot usage
- No alignment padding



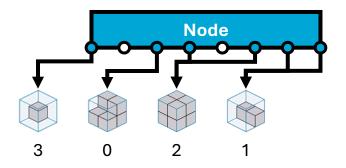


Ticket Board - Look-Up Efficiency



Look-ups require loading the entire slab from memory







Best of Both Worlds



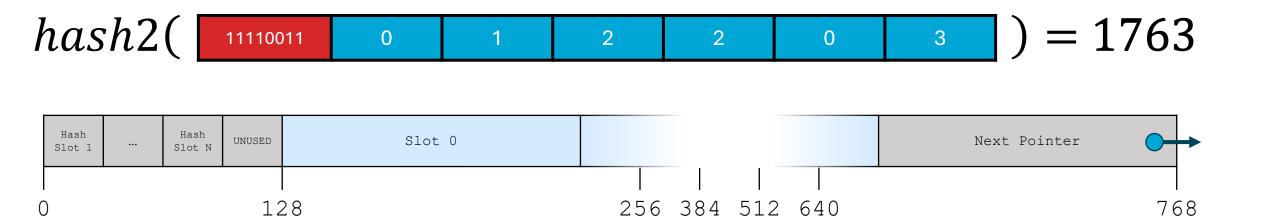
- Items are contiguous in memory (SVDAG traversal)
- Fast hash table look-ups
- Low memory overhead

Our solution: "acceleration hash"

Acceleration Hash (32-bit)



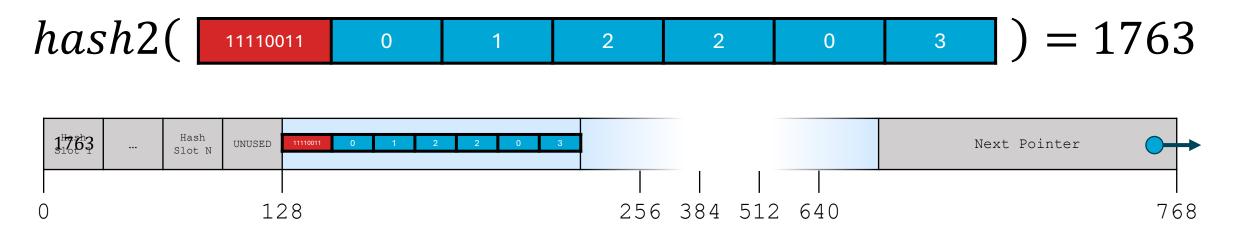
- 32-bit secondary hash of each slot
- Fast look-ups by first comparing secondary hash
- 31 slots per slab; aligned to cache line



Acceleration Hash (32-bit)



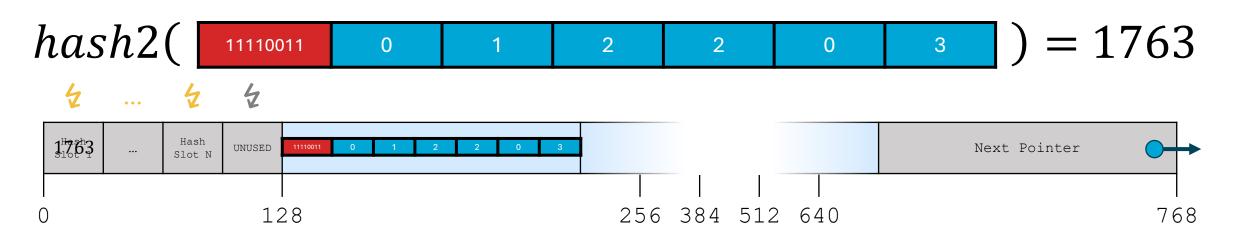
- 32-bit secondary hash of each slot
- Fast look-ups by first comparing secondary hash
- 31 slots per slab; aligned to cache line



Acceleration Hash (32-bit)



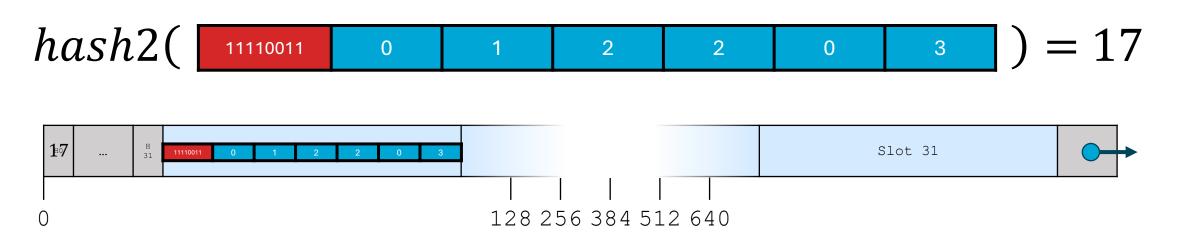
- 32-bit secondary hash of each slot
- Fast look-ups by first comparing secondary hash
- 31 slots per slab; aligned to cache line



Acceleration Hash (8-bit)



- 8-bit secondary hash to reduce memory overhead
- 32 slots per slab; no alignment padding





Evaluation

Evaluation



Implemented inside the HashDAG framework [CBE20]

Using the same test scenarios as previous work

Machine: Nvidia RTX4080, AMD 7950X3D, PopOS 22.04







Scene	Method	Memory
Citadel 128K³ (No Materials) SVO 15117 MiB SVDAG 980 MiB	Atomic U64	1199 MiB (+22.3%)
Citadel 128K ³ (With Materials)	Atomic U64	7164 MiB (+19.5%)
SVO 22516 MiB SVDAG 5997 MiB		
San Miguel 64K³ (With Materials)	Atomic U64	3509 MiB (+19.8%)
SVO 14865 MiB SVDAG 2929 MiB		
20201110		



Scene	Method	Memory
Citadel 128K³ (No Materials)	Atomic U64	1199 MiB (+22.3%)
SVO 15117 MiB SVDAG 980 MiB	Ticket Board	1155 MiB (+17.9%)
SVDAG 980 MID		
Citadel 128K³ (With Materials) SVO 22516 MiB SVDAG 5997 MiB	Atomic U64	7164 MiB (+19.5%)
	Ticket Board	7082 MiB (+18.1%)
SVDAG 5997 MID		
San Miguel 64K³ (With Materials)	Atomic U64	3509 MiB (+19.8%)
SVO 14865 MiB SVDAG 2929 MiB	Ticket Board	3461 MiB (+18.2%)
SVDAG 2929 MID		



Scene	Method	Memory
Citadel 128K³ (No Materials)	Atomic U64	1199 MiB (+22.3%)
SVO 15117 MiB SVDAG 980 MiB	Ticket Board	1155 MiB (+17.9%)
SVDAG 900 MID	Acceleration Hash (32-bit)	1400 MiB (+42.9%)
	Acceleration Hash (8-bit)	1203 MiB (+22.8%)
Citadel 128K³ (With Materials)	Atomic U64	7164 MiB (+19.5%)
SVO 22516 MiB SVDAG 5997 MiB	Ticket Board	7082 MiB (+18.1%)
SVDAG 5997 MID	Acceleration Hash (32-bit)	8685 MiB (+44.8%)
	Acceleration Hash (8-bit)	7404 MiB (+23.5%)
San Miguel 64K³ (With Materials)	Atomic U64	3509 MiB (+19.8%)
SVO 14865 MiB	Ticket Board	3461 MiB (+18.2%)
SVDAG 2929 MiB	Acceleration Hash (32-bit)	4269 MiB (+45.7%)
	Acceleration Hash (8-bit)	3622 MiB (+23.7%)





	Memory Usage	
64-bit Atomic	+	
Ticket Board	+	
32-bit Acceleration Hash	_	
8-bit Acceleration Hash	0	

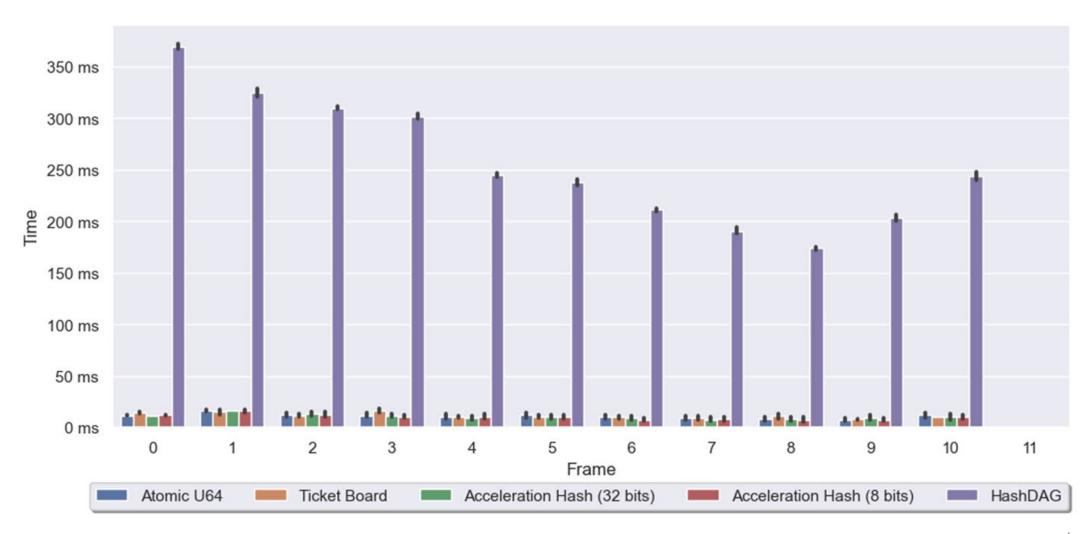


Editing Performance





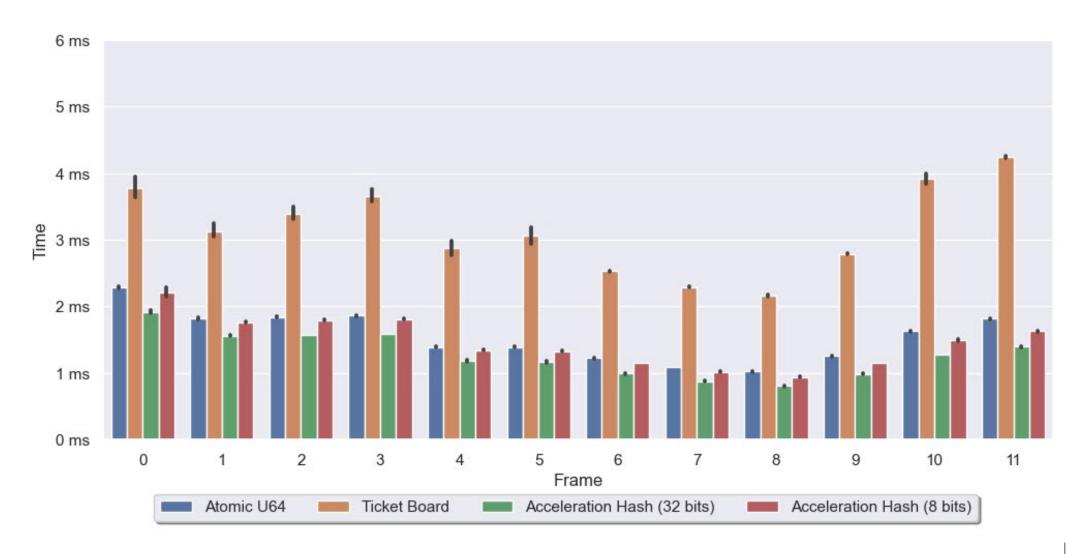
Frame Time (Without Materials)







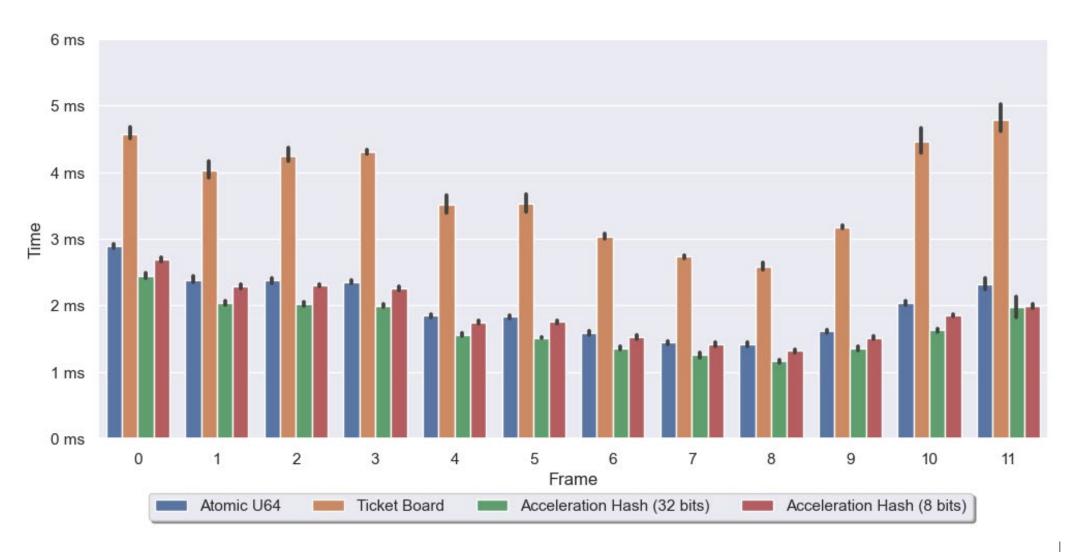
Merge SVO with SVDAG (Without Materials)





G)

Merge SVO with SVDAG (With Materials)









	Memory Usage	Editing
64-bit Atomic	+	+
Ticket Board	+	_
32-bit Acceleration Hash	_	+
8-bit Acceleration Hash	0	+



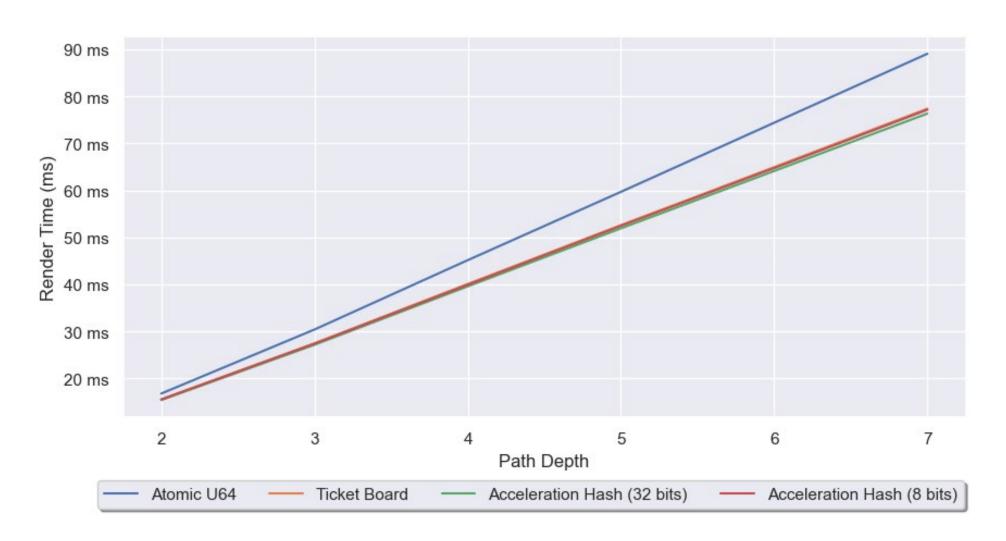
Rendering Performance

Path Tracing – Inside of Stanford Bunny 16K³



6

Path Tracing – Interior of Stanford Bunny 16K³







	Memory Usage	Editing	Ray Tracing
64-bit Atomic	+	+	0
Ticket Board	+	_	+
32-bit Acceleration Hash	_	+	+
8-bit Acceleration Hash	0	+	+





Most compact editing perfo	sage	Editing	Ray Tracing
64-bit Atomic	+	+	
Ticket Board	+	-	+
32-bit Acceleration Hash	-	+	+
8-bit Acceleration Hash		+	+

Fast rendering and editing, at the cost of memory usage.



Limitations & Future Work



- Using materials reduces SVDAG compression ratio significantly
- More advanced Garbage Collection



Closing Remarks



Details can be found in the paper & supplemental material

Planning to release the code on our website and GitHub:

https://publications.graphics.tudelft.nl/papers/13

https://github.com/mathijs727/

